Amendments to the Specification:

Please replace paragraph [0017] with the following amended paragraph:

[0017] FIG. 2 illustrates a schematic of a wide ratio current mirror circuit 200 in accordance with a first embodiment of the invention. The wide ratio current mirror circuit 200 comprises a first FET M1, a second FET M2, a third FET M3, a current sink 221 for sinking current Iin, a first bipolar transistor Q1 201, a second bipolar transistor Q2 202 and a load resistor ~~R1 231~~ 231. A first supply voltage port 200a is used for providing a positive supply voltage to the wide ratio current mirror circuit 200 and a second supply voltage port 200b is used for providing a negative, or ground, supply voltage to the wide ratio current mirror circuit 200.

Please replace paragraph [0019] with the following amended paragraph:

[0019] Transistors Q1 201 and Q2 202 form a current ratioing ~~circuit 206 circuit~~ circuit that includes a first portion disposed between the first current mirror port 205b and the second supply voltage port 200b and a second portion disposed between the first supply voltage port 200a and the second supply voltage port 200b, the second portion including a load current path that includes a load resistor 231. A current path is formed between the first supply voltage port 200a and the coupled base terminals of transistors Q1 201 and Q2 202. The current path includes a FET M3 213, with source and drain terminals disposed in series with the current path from the first supply voltage port 200a to coupled base terminals of transistors Q1 201 and Q2 202. The gate terminal of FET M3 213 is coupled with the second current mirror port 205a. Transistors Q1 201 and Q2 202 are formed so as to provide a statistical match with M times current ratio. The current flowing in the collector terminal of transistor Q2 202 is M times the current flowing in the collector terminal of transistor Q1 201. For the load current path, resistor ~~R1 231~~ 231 is disposed between the current ratio output port 206b and the first supply voltage port 200a.

Please replace paragraph [0020] with the following amended paragraph:

[0020] In equilibrium the drain current of FET M2 212 exactly balances the current Iin sinked through the current sink 221 and the potential on the drain terminal of FET M2 212 biases the gate terminal of FET M3 213. This causes current flow in the drain terminal of FET M3 213, which drives the base terminals of transistors Q1 201 and Q2 202. The resultant collector current in transistor Q1 201 drives the first current mirror port 205b and causes current to flow in the drain terminal of FET M2 212. By making FET M1 211 N times wider than FET M2 212 the current flowing in the collector terminal of Q1 201 is N times larger than the current flowing in the drain terminal of FET M2 212. By making transistor Q2 202 M times larger than transistor Q1 201 the current flowing in the collector terminal of Q2 202 is M times larger than the current flowing in the collector terminal of transistor Q1 201. Thus, the current propagating through the load resistor, R1, is M*N*Iin. Advantageously, FET devices, M1 211 and M2 212, have longer channels and have sufficient gate area to provide the statistical match, whereas FET M3 [[312]] 213 is a short channel device.

Please replace paragraph [0022] with the following amended paragraph:

[0022] FIG. 3 illustrates an implementation of a wide ratio current mirror circuit 300, in accordance with a second embodiment of the invention, for use in receiving of an RF input signal through a RF signal input port 300c. The wide ratio current mirror circuit 300 comprises a first transistor, in the form of a first FET M1 311, a second transistor, in the form of a second FET M2 312, a fifth transistor, in the form of a third FET M3 313, a first current sink 321 for sinking current Iin, a third transistor, in the form of a first bipolar transistor Q1 301, a fourth transistor, in the form of a second bipolar transistor Q2 302, a load resistor ~~R1 331~~ 331, resistors R2 332 R3 333 R4 334, and capacitors ~~C2 342 C1 341~~ 342 and 341. A first supply voltage port 300a is used for providing a positive supply voltage to the wide ratio current mirror circuit 300 and a second supply voltage port 300b is used for providing a negative, or ground, supply voltage to the wide ratio current mirror circuit 300.

Please replace paragraph [0024] with the following amended paragraph:

[0024] Transistors Q1 301 and Q2 302 form a current ratioing ~~circuit 306 circuit~~ circuit that includes a first portion disposed between the first current mirror port ~~305b~~ 305a and the second supply voltage port 300b and a second portion disposed between the first supply voltage port 300a and the second supply voltage port 300b, the second portion including a load current path that includes a load resistor 331. A current path is formed between the first supply voltage port 300a and the coupled base terminals of transistors Q1 301 and Q2 302. The current path includes the FET M3 313 and resistor R2 332 with source and drain terminals disposed in series with resistor R2 332 from the first supply voltage port 300a to coupled base terminals of transistors Q1 301 and Q2 302. The gate terminal of FET M3 313 is coupled with the second current mirror port 305a. Transistors Q1 301 and Q2 302 are formed so as to provide a statistical match with M times current ratio. The current flowing in the collector terminal of transistor Q2 302 is M times the current flowing in the collector terminal of transistor Q1 301. For the load current path, resistor ~~R1 331~~ 331 is disposed between the current ratio output port 306b and the first supply voltage port 300a. The base terminal of transistor Q1 301 is coupled with the base terminal of transistor Q2 302 through resistors R3 333 and R4 334 in series. A node is formed between resistors R3 333 and R4 334 is coupled with resistor R2 332 to the drain terminal of FET M3 313. The current sink 321 for sinking current Iin is disposed between the second supply voltage port 300b and the gate and drain terminals of FET M2 312 and the gate terminal of FET M3 313, respectively.

Please replace paragraph [0025] with the following amended paragraph:

[0025] A ~~capacitor C1~~ capacitor 341 is disposed between the gate and drain terminals of FET M3 313. Capacitor C2 342 is disposed between the RF input port 300c and the base terminal of transistor Q2 302 for capacitively coupling of the RF input signal thereto, where transistor Q2 302 is modulated through capacitor C2 342 by the RF input signal. Resistor R4 334 provides a DC potential to the base terminal of transistor Q2 302, where

resistor R3 333 provides a similar DC potential to the base terminal of transistor Q1 301. ~~Capacitor C1~~ capacitor 341 provides loop stabilization for FET M3 313 and resistor R2 332 aids in a pole split for the wide ratio current mirror circuit 300. Resistor R2 332 is used to isolate FET M3 313 from the resistively coupled base terminals of transistors Q1 301 and Q2 302. A voltage drop across resistor R3 333 matches the voltage drop across resistor R4 334.

Please replace paragraph [0026] with the following amended paragraph:

[0026] Miller feedback within the circuit is a result of the dominant pole formed by FET M3 313. A small change in current of FET M3 reflects back to gate terminal through capacitor C1 341, where resistor R2 332 and capacitor C1 341 operate in conjunction as a voltage swing reduction circuit to reduce large voltage swings on the gate terminal of FET M3 313. Opposite to that which is provided by the prior art illustrated in FIG. [[1a]] 1, which provides no stabilization correction.

Please delete paragraph [0033].

Please replace paragraph [0034] with the following amended paragraph:

[0034] Transistors Q1 401 and Q2 402 form a current ratioing ~~circuit 406 circuit~~ circuit that includes a [[first]] second portion disposed between the first current mirror port 405b and the second supply voltage port 400b and a second portion disposed between the first supply voltage port 400a and the second supply voltage port 400b, the second portion including a load current path that includes a load resistor 431. A current path is formed between the first supply voltage port 400a and the coupled base terminals of transistors Q1 401 and Q2 402. The current path includes the FET M3 413 and the resistor R3 433, with source and drain terminals disposed in series with resistor R3 433 along the current path from the first supply voltage port 400a to coupled base terminals of transistors Q1 401 and Q2 402. The gate terminal of FET M3 413 is coupled with the second current mirror port 405a. Transistors Q1 401 and Q2 402 are formed so as to provide a statistical

match with M times current ratio. The current flowing in the collector terminal of transistor Q2 402 is M times the current flowing in the collector terminal of transistor Q1 401.

Please replace paragraph [0035] with the following amended paragraph:

[0035] A first current mirror 405 is formed from FETs M1 411 and M2 412. Preferably, the FETs M1 411 and M2 412 are positive channel FETs (PFETs). The source terminals of the PFETs M1 411 and M2 412 are coupled to the first supply voltage port 400a. The gate terminals of the p channel FETs M1 411 and M2 412 are coupled together, coupled to the drain terminal of FET M1 411, and further coupled to the collector terminal of transistor Q1 401. A source terminal of FET M3 413 is coupled to the first supply voltage input 400a, with the gate terminal thereof coupled to the drain terminal of FET M2 412. A ~~second~~ first current mirror port 405a is formed at the drain terminal of FET M2 412 and a [[first]] second current mirror port 405b is formed at the drain terminal of FET M1 411.

Please replace paragraph [0036] with the following amended paragraph:

[0036]The current sink 421, for sinking of current Iin, is disposed between the second supply voltage port 400b and the second current mirror port 405a. A node formed between transistors Q1 401 and Q2 402 is coupled to the drain terminal of FET M3 413 via resistor ~~R3 432~~ R3 433 disposed in series. Source and drain terminals of FET M3 413 form a current path from the first supply voltage port 400a, via resistor R3 433, to coupled base terminals of transistors Q1 401 and Q2 402. Capacitor C1 441 is disposed between the gate and ~~source~~ drain terminals of FET M3 413 for providing loop stabilization for FET M3 413 and resistor R3 433 aids in a pole split for the circuits 400 and 450. Resistor R3 433 is used to isolate FET M3 413 from the coupled base terminals of transistors Q1 401 and Q2 402.

Please replace paragraph [0037] with the following amended paragraph:

[0037] Miller feedback within the circuit is a result of the dominant pole formed by FET M3 413. A small change in current of FET M3 413 reflects back to gate through capacitor C1 441, where resistor R3 433 and capacitor C1 441 operate in conjunction as a voltage swing reduction circuit to reduce large voltage swings on the gate terminal of FET M3 413. Opposite to that which is provided by the prior art illustrated in FIG. [[1a]] 1, which provides no stabilization correction.

Please replace paragraph [0038] with the following amended paragraph:

[0038] In equilibrium the drain current of FET M2 412 balances the current Iin from the current sink 421 and the potential on the drain terminal of FET M2 412 biases the gate terminal of FET M3 413. This causes current flow in the drain terminal of M3 413, which drives the base terminals of transistors Q1 401 and Q2 402. The resultant collector current in transistor Q1 401 drives the ~~first~~ second current mirror port 405b and causes current to flow in the drain terminal of FET M2 412. By making FET M1 411 N times wider than FET M2 412 the current in the collector terminal of transistor Q1 401 is N times larger than the current in the drain terminal of FET M2 412. By making transistor Q2 402 M times larger than transistor Q1 401 the current in the collector terminal of transistor Q2 402 is M times larger than the current in the collector terminal of Q1 401. Thus, the DC current propagating through the load, in the form of the differential amplifier 407, coupled between the second current ratio port 406b and the first supply voltage port 400a, is M*N*Iin, as shown. A second current source 422 is coupled to the base terminal of transistor Q2 402 and provides and offset current, Ioffset, thereto.

Please replace paragraph [0039] with the following amended paragraph:

[0039] The differential amplifier 407 comprises a differential bias port 407c coupled with the second current ratio output port ~~406b~~, 406b, a first bias port 407a, a second bias port 407b, and first and second RF signal input ports 400c and 400d in the form of differential RF input ports. A differential pair of seventh and sixth bipolar transistors Q3 403 and Q4

404, respectively, is disposed with coupled emitter terminals and coupled with the differential bias port 407c. ~~First and second~~ seventh and sixth load resistors, R1 431 and R2 432, are coupled in series between the collector ports of the first and second bipolar transistors Q3 403 and Q4 404, respectively, and the first supply voltage port 400a. A first bias resistor R4 434 is disposed between the first bias port 407a and the base terminal of transistor Q4 404. A second bias resistor R5 435 is disposed between the second bias port 407b and the base terminal of transistor Q3 403. The first and second bias ports, 407a and 407b, are coupled to the drain terminal of FET M3 413. A second capacitor C2 442 couples the first RF input port 400c to the base terminal of transistor Q4 404. A third capacitor C3 443 couples the second RF input port 400d to the base terminal of transistor Q3 403.

Please replace paragraph [0040] with the following amended paragraph:

[0040] Base terminal bias for transistors Q3 403 and Q4 404 is offset above the base terminal bias for transistor Q2 402 ~~because of by the~~ by the second current source 422 coupled to the base terminal of transistor Q2 402. Preferably transistor Q2 402 operates as close to saturation as possible in order to maximize the potential difference that is available to load, in the form of the differential amplifier 407.

Please replace paragraph [0047] with the following amended paragraph:

[0047] Further optionally, the PNP transistors ~~are used in order~~ can be used to replace FETs M1 211, 311, 411 and M2 212, 312, 412 and optionally FET M3 213, 313, 413. However, this is less desirable, especially for FET M3 213, 313, 413, because bipolar transistors, unlike FETs, have finite current gain.